UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,833	10/30/2003	Juing-Yi Cheng	TS02-150	9275

7590 09/03/2004

GEORGE O. SAILE
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
DANG, TRUNG Q	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,833	CHENG ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01/29/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 27, 30 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Segawa (U.S. Pat. 6,593,198).

With references to Figs. 1A, 2B and Embodiment 2, Segawa teaches the claimed invention in that Segawa discloses a method of manufacturing a gate electrode, comprising:

providing a substrate (1);

forming a patterned gate oxide (2) over said substrate;

forming a patterned gate material (3, 4, 5) over said patterned gate oxide;

forming a pair of LDD structures (6) in said substrate and respectively adjacent to said patterned gate oxide;

performing a plasma treatment to said patterned gate material and said substrate; and

respectively forming a pair of spacers (20B) over sidewalls of said patterned gate oxide and gate material.

Noted that the claim 27 employs "comprising" format, hence the last two steps are not necessarily performed in the sequence as recited.

For claim 30, see col. 9, lines 40-41 for the nitrogen based plasma treatment.

For claim 31, the annealing for activating dopants of source/drain regions (9) (col. 9, lines 33-35) reads on the claimed limitation because the annealing step as claimed is not necessarily performed immediately after the formation of the LDD structures.

3. Claims 1, 3, 4, 27, 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et al. (U.S. Pat. 6,323,519).

With reference to Figs. 1-4, Gardner teaches every limitation of the claimed invention in that Gardner discloses a method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate (12), the substrate having been provided with a patterned and etched layer of gate oxide (16) over the surface there-of and a patterned and etched layer of gate material (18) over said patterned gate oxide, a LDD impurity implant (14) into the substrate having been performed

and annealed self-aligned with the patterned and etched layer of gate material;

performing a plasma treatment (2) of the patterned and etched layer of gate material and exposed surfaces of the substrate; and

creating spacers (26) over sidewalls of the patterned and etched layer of gate material.

See col. 7, lines 40-41 for the LDD impurity implant regions (14) in the substrate that have been performed and annealed self-aligned with the patterned and etched layer of gate material. See col. 8, lines 45- 56 for the N2 based or O2 based plasma treatment of the patterned and etched layer of gate material and exposed surfaces of the substrate. Noted that the plasma treatment of the structure depicted in Fig. 2 is considered as a plasma treatment of the patterned and etched layer of gate material (18) and exposed surfaces of the substrate because it is believed that the surfaces of the substrate (12) and the sidewalls of the patterned polysilicon (18) are also nitridized (in the case of N2 based plasma) to some extend since there exists no layer at the interfaces between the thin oxide layer (22), the substrate and the polysilicon sidewalls (Fig.2) that would prevent activated nitrogen species in the plasma from permeating there-through . In the case of O2 based plasma, it is evident that oxygen species in the plasma penetrate through the abovementioned interfaces, which cause "additional oxide growth" (col. 8, lines

48-49). Notwithstanding the above reasoning, the "comprising" format of the claims does not exclude Gardner's process step for forming oxide layer (22).

Claim Rejections - 35 USC § 103

4. Claims 5-7, 9-13, 18-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. as above in view of Ueda (U.S. Pat. 6,387,735).

Gardner el. al. teach a method as noted in the above 102 (b) rejection, which further include the limitation "an active surface having been bounded over the substrate by creating regions of field isolation" (col. 7, lines 8-15) of independent claims 7, 18, 22 and 26.

Gardner differs from the claims in not disclosing limitations regarding: a) completing the gate electrode, including conductive interconnects there-to (claims 6, 7, 18, 22 and 26), and b) pocket implantation following LDD implantation (claims 5, 12, 20, 24, 26)

Ueda teaches a method for manufacturing a CMOS including a step of LDD implantation followed by a halo implantation (or pocket implantation) and a step of forming wiring electrodes (interconnects) after completion of the devices. See Fig. 2B and related text in which regions 5 are LDD implant regions and regions 6 are pocket implant regions. See col. 7, lines 60-61 and Fig. 1 for the step of forming interconnects.

It would have been obvious to one of ordinary skill in the art to modify the process of Gardner et al. by performing the pocket implantation following the LDD implantation as suggested by Ueda because it is within the level of one skilled in the art that pocket regions restrict the extent of a depletion region formed from heavily doped source and drain regions, hence reduce the risk of punchthrough. As for the formation of interconnects, it would have been obvious that metal interconnects to gate, source, and drain of the device are needed so as to put the device in practical use.

As for the limitation "performing a plasma treatment of the sidewalls of the gate electrode and the exposed substrate" of claims 7, 18, 22 and 26, Gardner 's reference reads on the claimed limitation for the same reasons noted in the above 102(b) rejection.

As for claim 26, see col. 7, lines 47-50 in Ueda for the step of annealing the LDD and pocket impurity implants.

5. Claims 2, 4, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. in view of Saul et al. (U.S. Pat. 5,425,843).

Gardner et al. teach a method as noted in the above 102(b) rejection, including a LDD implantation followed by an annealing self-aligned with the patterned and etched layer of gate material (col. 7, lines 40-41).

Gardner et al. differ from the claims in not disclosing the claimed limitation regarding a H2 based plasma treatment of the patterned and etched layer of gate material and the exposed surface of the substrate.

Saul et al. recognize that etching of a silicon dioxide layer grown and/or deposited on an underlying silicon substrate causes lattice damage to the substrate (col. 1, lines 31- 36). Accordingly, Saul et al. teach a process for post etching treatment of a damaged semiconductor device, which process includes plasma treating a semiconductor structure having an etched pattern therein with a plasma comprising H2 and N2 (col. 2, lines 5-11, lines 52-64; col. 3, lines 51-56).

Thus, in light of Saul ' s teaching, one of ordinary skill in the art would readily recognize that the etching of the gate layer (18) and oxide layer (16) in Gardner (see Fig.1) would cause lattice damage to the underlying silicon substrate (12). Therefore, one skilled in the art would find it obvious to modify the teaching of Gardner et al. by performing a plasma treatment of the structure of Fig. 1 in a plasma comprising H2 and N2 because the plasma treatment would reduce the amount of damage to the silicon substrate, hence reducing problems associated with the device performance.

6. Claims 7, 8, 10-17, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. taken with Saul et al. as applied to claims 2, 4, 28 and 30 above, and further in view of Ueda cited above.

The combination of Gardner et al. and Saul et al. teach the method as described in the above 103(a) rejection.

The combined teaching differs from the claims in not disclosing limitations regarding: a) completing the gate electrode, including conductive interconnects there-to (claims 7, 14, 22 and 26), and b) LDD implantation followed by pocket implantation (claims 12, 16, 24 and 26).

Ueda teaches a method for manufacturing a CMOS including a step of LDD implantation followed by a halo implantation (or pocket implantation) and a step of forming wiring electrodes (interconnects) after completion of the devices. See Fig. 2B and related text in which regions 5 are LDD implant regions and regions 6 are pocket implant regions. See col. 7, lines 60-61 and Fig. 1 for the step of forming interconnects.

It would have been obvious to one of ordinary skill in the art to modify the combined process of Gardner et al. and Saul et al. by performing the pocket implantation following the LDD implantation as suggested by Ueda because it is within the level of one skilled in the art that pocket regions restrict the extent of a depletion region formed from heavily doped source and drain regions, hence reduce the risk of punchthrough. As for the formation of interconnects, it would have been obvious that metal interconnects to gate, source, and drain of the device are needed so as to put the device in practical use.

As for claim 26, see col. 7, lines 47-50 in Ueda for the step of annealing the LDD and pocket impurity implants.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

8/25/04